UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/741,195	12/21/2000	Toshiyuki Hirota	040373/0300	7014

22428 7590 01/30/2003

FOLEY AND LARDNER
SUITE 500
3000 K STREET NW
WASHINGTON, DC 20007

EXAMINER
VU, QUANG D

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 01/30/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/741,195	HIROTA ET AL.	
	Examiner	Art Unit	
	Quang D Vu	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *amendment filed on 11/06/02* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,6-9,11-16,18-23 and 25-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *18-23 and 28* is/are allowed.

6)☒ Claim(s) *1-4,6-9,11-16,25-27 and 29-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claims 29-32 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Claims 29-32, in lines 1-10, the phrase "...comprising the steps of: a) planarizing a top surface of the interlayer insulating film; b) forming an oxide film on the planarized top surface of the interlayer insulating film; and c) in the high density region, masking the oxide film in a particular pattern using a fluorine-based resist, wherein the steps a), b) and c) are performed in sequence between the step of forming the interlayer insulating film and the step of annealing in an atmosphere containing water vapor" is not supported by the original specification. The specification only discloses the steps a), b) and c) after the step of annealing in an atmosphere containing water vapor.

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 6-9, 26 and 30 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 6, in line 10, the phrase "...masking the high density region of the semiconductor substrate..." is unclear. The specification (figs. 18A, 18B) discloses etching the first nitride film in only the low-density region to expose the gate oxide film in gaps between the gate electrodes and also to expose the nitride protective films on the gate electrodes without masking the high-density region of the semiconductor substrate. The specification never discloses masking the high-density region of the semiconductor substrate, and then etching the first nitride film in only the low-density region to expose the gate oxide film in gaps between the gate electrodes and also to expose the nitride protective films on the gate electrodes.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1 – 4, 25, 11 – 16 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 6,326,270 to Lee et al.

Regarding claim 1, Lee et al. (figures 3A-G, 5) teach a method of manufacturing a semiconductor device having, on a single semiconductor substrate, a high-density region (cell array region) containing transistor elements arrayed at a high density and a low-density region

(peripheral circuit region) containing transistor elements arrayed at a low density, comprising the steps of:

forming a gate oxide film (column 7, lines 25-26) on a surface of the semiconductor substrate (100);

forming gate electrodes (104, 105) on a surface of the gate oxide film, and forming oxide film (110) on the gate electrodes (104, 105);

uniformly forming a first nitride film (112) having a predetermined thickness on the surface with the gate electrodes (104, 105) formed thereon;

masking the high density region of the semiconductor substrate (100), and etching the first nitride film (112) in only the low density region to expose the gate oxide film (110) in gaps between the gate electrodes (104, 105);

uniformly forming a second nitride film (119) having a predetermined thickness on the surface on which the first nitride film (112) is etched;

forming an interlayer insulating film (120) on the second nitride (119) with an impurity introduced therein on a surface of the second nitride film (column 8, lines 39-40).

self-aligning the high-density region using the first nitride film (112) positioned on sides of the gate electrodes (104, 105) as an etching stopper to form contact holes (124) reaching the semiconductor substrate (100) in the interlayer insulating film (120), wherein all portions of the second nitride film (119) that are in direct contact with the first nitride film (112) positioned on sides of the gate electrodes (104, 105) are removed as a result of the self aligning step;

forming contact electrodes (126) connected to the semiconductor substrate (100) in the contact holes (124) (see figures 3A-G, 5).

It is inherent that annealing an assembly formed so far with a forming gas to recover an interfacial level.

Lee et al. differ from the claimed invention by not showing annealing an assembly formed so far in an atmosphere containing water vapor. It would have been obvious to one having ordinary skill in the art at the time the invention was made for annealing an assembly formed so far in an atmosphere containing water vapor, since it is common in the art to perform annealing steps to repair substrate damage, activate dopants, form silicide and other reasons. Additionally, it is also to perform annealing steps at any time during fabrication.

Regarding claim 2, Lee et al. differ from the claimed invention by not showing the first nitride film and the second nitride film is formed by a CVD. Lee et al. is silent with respect to how the nitride film is deposited. One having ordinary skill in the art would have been required to select a known method of deposition. It would have been obvious to select CVD, since it is a well-known method.

Regarding claim 3, Lee et al. teach a method, wherein the thickness of the first and second nitride films are formed to a thickness of about 20 –200 Angstroms (2-20 nm) (column 8, lines 1-3) and 50-150 Angstroms (5-15nm) (column 9, lines 37-38), respectively. Lee et al. teach a method, wherein the second nitride film is formed to a thickness ranging from 3.0 to 20 nm. Lee et al. do not teach a method, wherein the first nitride film is formed to a thickness ranging from 30 to 50 nm. It would have been obvious to one having ordinary skill in the art at the time of the invention was made for the first nitride film is formed to a thickness ranging from 30 to 50 nm, since it has been held that where the general conditions of a claim are disclosed in the prior

art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

Regarding claim 4, Lee et al. teach a method, wherein the first nitride film (112) is formed to a thickness large enough to serve as an etching stopper for self-aligning the high-density region.

It is inherent that the second nitride film is formed to a thickness which prevents an impurity of the interlayer insulating film from being diffused into the semiconductor substrate by annealing the assembly in the atmosphere containing the water vapor and also prevents the semiconductor substrate from being oxidized by annealing the assembly in the atmosphere containing the water vapor, but allow the forming gas to be diffused into the semiconductor substrate.

Regarding claim 25, Lee et al. teach a method, wherein the second nitride film (119) only remains directly beneath the interlayer insulating film (120) after the self-aligning step is completed.

Regarding claim 11, Lee et al. (figures 3A-G, 5) teach a method of manufacturing a semiconductor device having, on a single semiconductor substrate, a high-density region containing transistor elements arrayed at a high density and a low-density region containing transistor elements arrayed at a low density, comprising the steps of:

forming a gate oxide film on a surface of the semiconductor substrate (100);

forming gate electrodes (104, 105) on a surface of the gate oxide film, forming oxide films on the gate electrodes;

uniformly forming a first nitride film (112) having a predetermined thickness on the surface with the gate electrodes (104, 105) formed thereon;

etching the first nitride film (112) and gate oxide to expose the substrate (100) in gaps between gate electrodes (104, 105) in said in the low-density region;

uniformly forming a second nitride film (119) having a predetermined thickness on the surface on which the oxide film (110) is etched;

forming an interlayer insulating film (120) on the second nitride (119) with an impurity introduced therein on a surface of the second nitride film (119) (column 8, lines 39-40).

self-aligning the high-density region using the first nitride film (112) positioned on sides of the gate electrodes (104, 105) as an etching stopper to form contact holes (124) reaching the semiconductor substrate (100) in the interlayer insulating film (120), wherein all portion of the second nitride film (119) that are in direct contact with the first nitride film (112) positioned on sides of the gate electrodes (104, 105) are removed as a result of the self aligning step;

forming contact electrodes (126) connected to the semiconductor substrate (100) in the contact holes (124) (see figures 3A-G, 5).

It is inherent that annealing an assembly formed so far with a forming gas to recover an interfacial level.

Lee et al. differ from the claimed invention by not showing annealing an assembly formed so far in an atmosphere containing water vapor. It would have been obvious to one having ordinary skill in the art at the time the invention was made for annealing an assembly formed so far in an atmosphere containing water vapor, since it is common in the art to perform annealing

steps to repair substrate damage, activate dopants, form silicide and other reasons. Additionally, it is also to perform annealing steps at any time during fabrication.

Regarding claim 12, Lee et al. differ from the claimed invention by not showing the first nitride film and the second nitride film is formed by a CVD. Lee et al. is silent with respect to how the nitride film is deposited. One having ordinary skill in the art would have been required to select a known method of deposition. It would have been obvious to select CVD, since it is a well-known method.

Regarding claim 13, Lee et al. teach a method, wherein the thickness of the first and second nitride films are formed to a thickness of about 20 –200 Angstroms (2-20 nm) (column 8, lines 1-3) and 50-150 Angstroms (5-15nm) (column 9, lines 37-38), respectively. Lee et al. teach a method, wherein the second nitride film is formed to a thickness ranging from 3.0 to 20 nm. Lee et al. do not teach a method, wherein the first nitride film is formed to a thickness ranging from 30 to 50 nm. It would have been obvious to one having ordinary skill in the art at the time of the invention was made for the first nitride film is formed to a thickness ranging from 30 to 50 nm, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

Regarding claim 14, Lee et al. do not teach a method, wherein the first nitride film is formed by a chemical vapor deposition process, and the second nitride film is formed by a rapid thermal nitriding process. Lee et al. is silent with respect to how the first nitride film is deposited. It would have been obvious to select CVD, since it is a well-known method. Rapid

thermal nitriding is a well known a method of forming nitride layer. It would have been obvious to select rapid thermal nitriding, since it is a well-known method.

Regarding claim 15, Lee et al. teach a method, wherein the second nitride film is formed to a thickness of 2.0 nm (20 Angstroms; column 8, lines 1-3). Lee et al. differ from the claimed invention by not showing a method, wherein the first nitride film is formed to a thickness ranging from 30 to 50 nm. It would have been obvious to one having ordinary skill in the art at the time of the invention was made for the first nitride film is formed to a thickness ranging from 30 to 50 nm, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

Regarding claim 16, Lee et al. teach a method, wherein the first nitride film is formed to a thickness large enough to serve as an etching stopper for self-aligning the high-density region.

It is inherent that the second nitride film is formed to a thickness which prevents an impurity of the interlayer insulating film from being diffused into the semiconductor substrate by annealing the assembly in the atmosphere containing the water vapor and also prevents the semiconductor substrate from being oxidized by annealing the assembly in the atmosphere containing the water vapor, but allow the forming gas to be diffused into the semiconductor substrate.

Regarding claim 27, Lee et al. teach a method, wherein the second nitride film (119) only remains directly beneath the interlayer insulating film (120) after the self-aligning step is completed.

Allowable Subject Matter

7. Claims 18-23 and 28 are allowed.

8. The following is an examiner's statement of reasons for allowance: The most closely related art, US Patent No. 6,326,270 to Lee et al. Lee et al. do not anticipate or render the claimed invention such as etching the first nitride film in only the low-density region expose the nitride protective films on the gate electrodes.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Response to Arguments

Applicant's arguments with respect to claims 1-4 and 11-16 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quang D Vu whose telephone number is 703-305-3826. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 703-308-2772. The fax phone numbers for the

organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

qv
January 27, 2003

Steven Loke